

REMARKS

I. Introduction

Applicants would like to thank Examiner Lam for the indication of allowable subject matter recited by claims 4-8 and 12-24. In response to the Office Action dated November 8, 2004, Applicants have amended Fig. 16 in the manner suggested by the Examiner to include the legend "Prior Art." Additionally, Applicants have canceled claims 1-3 and 9-11, without prejudice or disclaimer. Applicants have also rewritten claims 4 and 12 into independent format, and amended claims 4-7, 12 and 17 so as to further clarify the claimed subject matter and to address the pending rejection under 35 U.S.C. § 112, second paragraph. New claims 25-42 are added. Support for these amendments can be found, for example, in Figs. 1-4 and 6, and their corresponding sections of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-24 Under 35 U.S.C. § 112, Second Paragraph

Claims 1-24 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. As discussed above, claim 1 has been canceled, thus rendering the rejection thereof moot. Claims 4 and 12 have been amended to incorporate the claim elements recited by claim 1. Applicants respectfully submit that claims 4 and 12 comply with the requirements of 35 U.S.C. § 112, second paragraph.

Specifically, in the pending rejection, the Examiner asserts that the delay selecting section selects and outputs one of the plurality of delayed pulse signals, as shown in Fig. 1 of

Applicants' drawings. The Examiner then concludes that the delay selecting section does not generate a plurality of delayed output data pieces, and select and output one of the delayed output data pieces.

Applicants respectfully submit that the foregoing claimed subject matter is disclosed, for example, at page 12, lines 12-16 of the specification. Specifically, the delay selecting section 105 sequentially delays the latch pulse signal s104c from the read control section 104 using the delay circuits 1051 through 105n, and generates a plurality of delayed pulse signals (e.g., output of 1051, output of 1052 and output of 105n) having mutually different delay amounts. Then, the delay selecting section 105 selects and outputs one of the outputs (e.g., A') from the delay circuits 1051 through 105n using the selection part 105a. Thus, contrary to the conclusion set forth by the Examiner, the delay selecting section generates a plurality of delayed output data pieces, and selects and outputs one of the delayed output data pieces.

Additionally, the claim elements recited by claims 4 and 12 are directed to the second embodiment of the present invention, rather than to the first embodiment of the present invention. As indicated in Fig. 8 of Applicants' drawings, the delay selecting section 105 also delays the output data with a plurality of delay amounts (e.g., via 1051, 1052 and 105n), and generates a plurality of delayed output data pieces (e.g., output of 1051, output of 1052 and output of 105n). Given these delayed output data pieces, the delay selecting section 105 then selects and outputs one of the delayed output data pieces (e.g., B') to the latch circuit 106.

Furthermore, the Examiner asserts that the claim limitation "a latch circuit for receiving the delayed output data piece selected by the delay selecting section and a latch pulse signal" is indefinite, because the latch circuit 106 of Fig. 1 only receives data pieces from the memory 100 and the selected one of the delayed pulse signals. The Examiner then concludes that the latch

circuit does not receive the delayed output data piece selected by the delay selecting section and the latch pulse signal.

However, as disclosed in Fig. 8 and at page 22, lines 14-16 of the specification, the latch pulse signal s104c output from the read control section 104 is input to the latch circuit 106, such that the latch circuit 111 receives the delayed output data piece (e.g., B') selected by the delay selecting section 105 and the latch pulse signal s104c. As such, contrary to the Examiner's assertion, it is clear that the latch circuit 106 receives the delayed output data piece selected by the delay selecting section 105 and the latch pulse signal s104c. For the foregoing reasons, it is respectfully submitted that the scope of the pending claims would be readily understood by those of skill in the art when read in light of the specification, and therefore claims 4 and 12 are fully compliant with the requirements of 35 U.S.C. § 112, second paragraph.

With respect to claims 5-7, the Examiner asserts that the claim term "if" is indefinite, because it is not a positive recitation. Although the Applicants do not agree with the Examiner's interpretation, in an effort to advance prosecution, claims 5-7 have been amended in the manner suggested by the Examiner. It is respectfully submitted that claims 5-7, as amended, comply with the requirement of 35 U.S.C. § 112, second paragraph.

With respect to claims 10 and 11, the Examiner asserts that the claim limitation "the latch circuit is provided in a second LSI" recited by claim 10 is indefinite, while the claim phrase "the first LSI" lacks proper antecedent basis. In response, Applicants have canceled claims 10 and 11, thus rendering the rejection to claims 10 and 11 moot.

With respect to claims 15 and 17, the Examiner asserts that the claim limitation "the latch circuit latches the output data at rising and falling edges of the latch pulse signal" is indefinite,

because the latch circuit 106 only latches the data pieces from the memory in response to the selected delayed latch pulse signal.

However, as discussed above and as illustrated in Figs 8 and 9, the latch circuit 111 may also latch the output data in accordance with the latch pulse signal s104c. Thus, for this reason, it is respectfully submitted that claims 15 and 17 are clear and unambiguous.

For all of the foregoing reasons, it is respectfully submitted that the foregoing amendments to the claims, in conjunction with the foregoing explanation, which identifies the relevant portions of the specification that support the claim terms questioned in the pending rejection, overcome the pending rejection under 35 U.S.C. § 112, second paragraph.

III. The Rejection Of Claims 1-2 and 9-11 Under 35 U.S.C. § 102

Claims 1-2 and 9-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by USP No. 5,022,056 to Henderson. In response, Applicants have canceled claims 1-2 and 9-11, without prejudice or disclaimer. Thus, the pending rejections to claims 1-2 and 9-11 are moot in view of the cancellation thereof.

Furthermore, as new claim 25 includes the allowable features “comparison circuit” and “determination section” indicated by the Examiner (see, “Allowable Subject matter” of Office Action), it is respectfully requested that claim 25 be allowed.

Moreover, it does not appear that any of the cited references discloses or suggests the claim elements recited by new claim 30. Thus, it is respectfully submitted that new claim 30 is patentably distinct over the cited prior art.

IV. **All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable**

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 4, 12, 25 and 30 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

V. **Conclusion**

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Application No.: 10/715,538

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/AHC
Facsimile: 202.756.8087
Date: February 7, 2005

**Please recognize our Customer No. 20277
as our correspondence address.**

Application No.: 10/715,538

IN THE DRAWINGS

Please amend Fig. 16 as indicated on the enclosed copy thereof. Fig. 16 has been amended to include the legend "Prior Art."